WHAT IS CLAIMED IS:

1. A method of forming GaAs distributed Bragg reflector, comprising:

forming an InP layer;

growing a fast GaAs layer on the InP layer at a temperature of between 400-450 °C;

growing a second GaAs layer on the fast GaAs layer at a temperature of about 600 °C; and

forming a GaAs/Al(Ga)As distributed Bragg reflector on the second GaAs layer.

2. A method of forming a GaAs distributed Bragg reflector according to claim 1, wherein the fast GaAs seed layer is grown using MOCVD.

3. A method of forming a GaAs distributed Bragg reflector according to claim 1, wherein the fast GaAs seed layer is grown to a thickness of between 20 and 40 nanometers.

4. A method of forming a GaAs distributed Bragg reflector according to claim 1, further including forming an insulation layer over the second GaAs layer, the insulation layer including an opening to the second GaAs layer, and the insulation layer is overgrown with a lateral epitaxial overgrowth.

5. A method of forming a GaAs distributed Bragg reflector according to claim 4, wherein the insulation layer is comprised of silicon oxide.

6. A method of forming a GaAs distributed Bragg reflector according to claim 4, wherein the insulation layer is comprised of silicon nitride.

7. A vertical cavity surface emitting laser, comprising:

an InP layer;

a first GaAs layer on said InP layer, wherein said first GaAs layer is formed by MOCVD at a temperature between 400-450 °C; and

a second GaAs layer on said first GaAs layer, wherein said second GaAs layer is formed by MOCVD at a temperature of around 600 °C.

8. A vertical cavity surface emitting laser according to claim 7, further comprising a GaAs/Al(Ga)As distributed Bragg reflector on said second GaAs layer.

9. A vertical cavity surface emitting laser according to claim 8, further including an insulation layer over said second GaAs layer, said insulation layer having an opening to said second GaAs layer, wherein said GaAs/Al(Ga)As distributed Bragg reflector is grown on said insulation layer using a lateral epitaxial overgrowth.

10. A vertical cavity surface emitting laser according to claim 9, wherein said InP layer is a spacer.

11. A vertical cavity surface emitting laser according to claim 7, wherein said first GaAs layer is between 20 and 40 nanometers thick.

12. A vertical cavity surface emitting laser, comprising:

an InP substrate;

a lower DBR over said InP substrate;

a bottom InP spacer over said lower DBR;

an InP active layer over said bottom InP spacer;

a top InP spacer over said InP active layer;

a first GaAs layer on said top InP spacer, wherein said first GaAs layer is formed by MOCVD at a temperature between 400-450 °C; and

a second GaAs layer on said first GaAs layer, wherein said second GaAs layer is formed by MOCVD at a temperature of around 600 °C.

13. A vertical cavity surface emitting laser according to claim 12, further including a GaAs/Al(Ga)As DBR mirror stack on said second GaAs buffer layer.

14. A vertical cavity surface emitting laser according to claim 13, further including an insulating structure on said second GaAs buffer layer, wherein said insulating structure includes an opening.

15. A vertical cavity surface emitting laser according to claim 14, wherein said GaAs/Al(Ga)As DBR mirror stack is grown over said insulating structure by lateral epitaxial overgrowth.

16. A vertical cavity surface emitting laser according to claim 15, further including a tunnel junction between said InP active layer and said top InP spacer.

17. A vertical cavity surface emitting laser according to claim 16, wherein said tunnel junction is comprised of MOCVD-grown $GaAs_{(1-x)}Sb_x$.

18. A vertical cavity surface emitting laser according to claim 12, wherein said first GaAs layer is between 20 and 40 nanometers thick.

19. A vertical cavity surface emitting laser according to claim 12, wherein said lower DBR and said GaAs/Al(Ga)As DBR mirror stack are of different material systems.

20. A vertical cavity surface emitting laser according to claim 14, wherein said insulating structure includes SiO_2 or Si_2N_4.